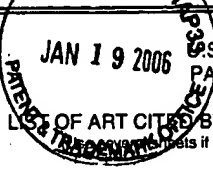



Form PTO-1449					ATTY. DOCKET NO. MI22-1660		SERIAL NO. 09/810,595	
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE LIST OF ART CITED BY APPLICANT <small>(Indicate relevant documents if necessary)</small>					APPLICANT: Belford T. Coursey			
					FILING DATE 03/15/2001		GROUP 2813	
U.S. PATENT DOCUMENTS								
*Examiner's Initials	Class	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate	
JLM	AA	5,933,726	08/99	Nishimura et al.	—	—		
	AB	6,015,983	01/00	Parekh	—	—		
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	AI							
FOREIGN PATENT DOCUMENTS								
		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AK							
	AL							
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)								
JLM	AM		Wolf, <i>Silicon Processing For The VLSI Era, Vol. 2: Process Integration</i> , Lattice Press, pp. 238 (1990).					
	AN							
	AO							
EXAMINER 		DATE CONSIDERED 4/16/06						
<small>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</small>								

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U.S. PATENT DOCUMENTS

Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
<i>JMM</i>	AA	5,396,093	3/1995	Lu	—	—	—
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	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AJ							
	AK							
	AL							

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

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EV550714900

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